Compact Receivers and Smart-Pixel Chips for Optical 1 nterconnects and Signal Processing

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ABSTRACT

A continuous-time shift-invariant cellular neural network (CNN) with hardware annealing capability, digitally programmable synaptic weights, and optical inputs/outputs has been developed. This electro-optical neurocomputing processor has great potential in solving many important scientific problems in signal processing and optimization. Advanced packaging for the proposed optoelectronic neurocomputing system is a thin-film silicon-substrate multichip module with flip-chip connection technologies. This paper presents two functional chips designed for the proposed electro-optical neurocomputing processor: a monolithic GaAs 2-D array of optical receivers, and a VLSI CMOS 2-D array of smart pixels based on the annealed CNN. Due to the multichip module integration of these chips in the same silicon substrate, a complete optoelectronics neurocomputing system can be realized in a very compact hardware.

Keywords: array processors, multichip module, neural networks, optical interconnection, optoelectronic integrated circuit, photodetectors, smart pixels, VI .S1 system

1. INTRODUCTION

A cellular neural network (CNN) is a locally connected, massively paralleled computing system with simple synaptic operators so that it is very suitable for Vi .SI implementation in real-time, high-speed applications. Several structural variations of the continuous-time, shift invariant, rectangular-gird network which was introduced by Chua and Yang [1,2] in 1988, have been reported, Among them are discrete-timc CNN and CNNS with nonlinear and delay-type templates [3]. VLSI implementation of discrete- or continuous-time CNNS have been studied by many researchers [4] - [8] Under the mild conditions [1], a CNN autonomously finds a stable solution for which the Lyapnov function of the network is locally minimized. The CNN can be used in many computation-intensive applications such as image and signal processing, Moreover, the quadratic nature of the Lyapnov function allows its applicability into optimization problems [9].

Figure 1 shows a system diagram of a multistage neural network based on optoelectronic approach [10]. Optical interconnection and optoelectronic neurocomputing systems can take the combined advantages of the optics and electronics. In order to achieve a reliable implementation for an optoelectronic integrated computing system, the fabrication and packaging technology should be well supported for the optical functions as well as the electrical functions.

in this paper,a continuous-time shift-invariant CNN with hardware annealing capability, digitally programmable synaptic weights, and optical input s/outputs is presented. The proposed CNN has more significant features than the basic CNN:

(A) To improve the local minimized energy function of the basic CNN, the annealing capability is included to accommodate the applications in which the optimal solutions of energy function are needed. Hardware annealing, [11] which is a paralleled version of effective mean-field annealing in analog net works, is a highly efficient method of finding optima] solutions for cellular neural networks.

(B) To improve the fixed synapse weights of the basic CNN, the digitally programmable synapse weights arc designed for the annealed CNN to accommodate the appl i cat ions in which programmable pre-determined operators are needed [12].

(C) To improve the global interconnections and external image 1/0 of the basic CNN, a 2-D array of optical receivers and transmitters is integrated with the annealed CNN to accommodate the applications in which high-speed parallel external image 1/0 and optical interconnections are needed [13].

This electro-optical neurocomputing processor has great potential in solving many important scientific problems in signal processing and optimization by the usc of the improved CNN with programmable pre-determined synaptic weights, hardware annealing capability, and parallel 2-D optical I/O ports. Advanced packaging for the proposed optoelectronic neurocomputing system is a thin-film silicon-substrate multichip module with flip-chip connection technologies such as the thermal-compression bonding [14, 15]. A compact multi-chip module of integrated 2-D array of optical receivers and smart-pixels as shown in Fig. 2 can take the combined advantages of the optics and electronics and achieve high-speed computer communication and signal processing. Figure 2a shows an optoelectronic neurocomputer based on the annealed CNN using planar optics and flip-chip connected multichip module packaging. Figure 2b shows a 3-D free-space optical interconnected optoelectronic neurocomputer based on the annealed CNN with 3-D multichip module or chip stack packaging. Two functional chips for the proposed electro-optical ncurocomputing processor based on the annealed CNN have been designed, fabricated, and tested: (A) a monolithic GaAs 2-D array of optical receivers, and (B) a VLSI CMOS 2-D array of smart pixels based on the annealed CNN. Due to the multichip module integration of these chips in the same silicon substrate, a complete optoelectronics neurocomputing system can be realized in a very compact hardware, Section two presents the theory, architecture, detailed circuit design, and chip implementation for the 2-D array of smart pixels design based on the annealed cellular neural network. Section three describes the optical receiver design, simulation, implementation, and measurement in details. Section four gives a conclusion.

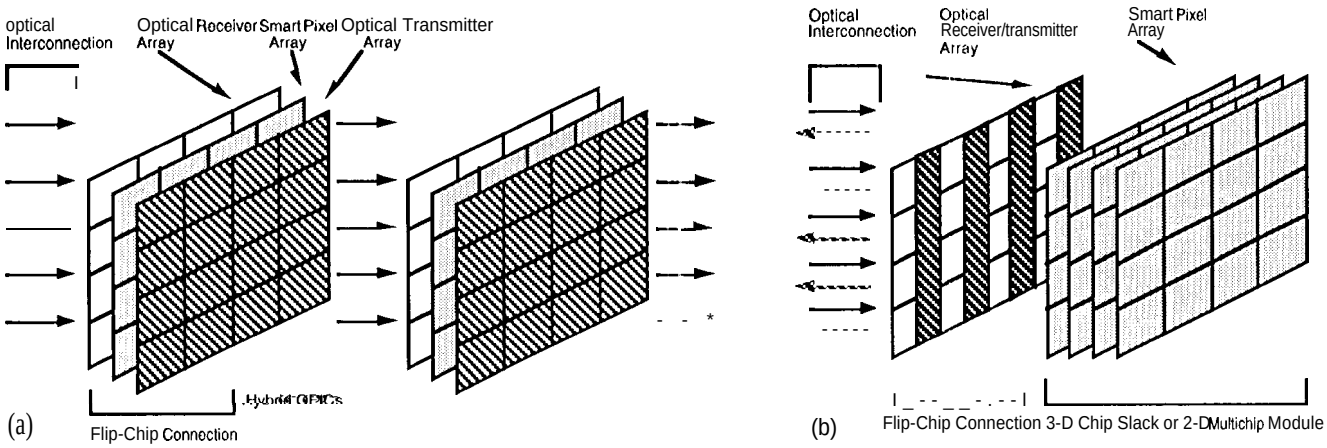


Fig. 1. Multistage communication-computation neural networks using the optoelectronic approach:
(a) Using unidirectional optical 1/0, (b) Using hi-directional optical 1/0.

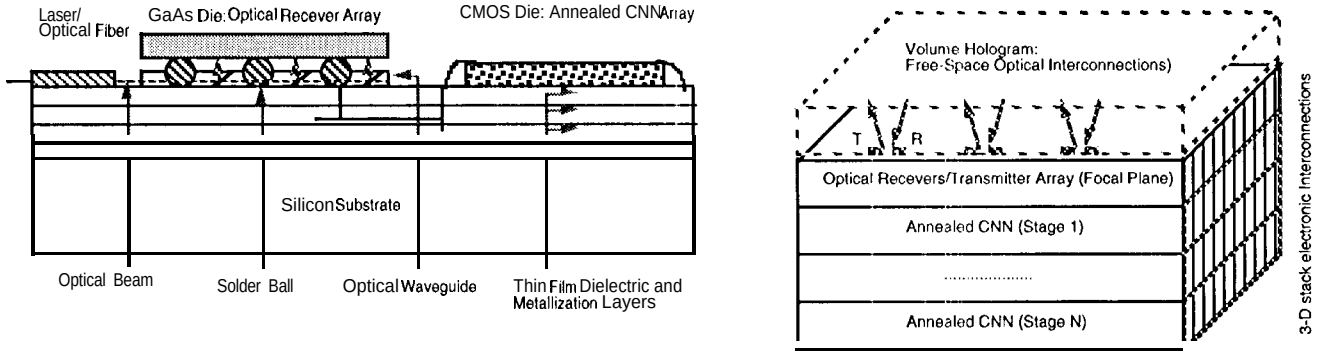


Fig. 2. An optical interconnected optoelectronic neurocomputer multichip module:
(a) Using planar optics and fiber links. (b) Using free-space optical interconnections.

2. A VLSI 2-D ARRAY OF SMART PIXELS BASED ON THE ANNEALED CNN

A VLSI 2-D array of smart pixels have been developed based on cellular neural networks with annealing ability. The experimental CMOS chip design of a continuous-time shift-invariant CNN with r = 1 is considered. For the maximum flexibility over a variety of applications, CNN circuits with hardware annealing capability and digitally programmable synaptic weights are designed and verified via circuit simulation. The proper network operation is confirmed for known and arbitrary cloning templates.

2.1. Cellular Neural Networks with Annealing: Theory

Consider an annealed CNN with n x m neurons. Each neuron has the piecewise-linear transfer function $f_{pw}(.)$ and its gain is variable as shown in Fig. 3. The gain is controlled by a monotonically increasing function g(t) such that

$$v_y = f_{pw}(g v_x) = \begin{cases} +1, \text{ if } v_x > \frac{1}{g} \\ g v_x, \text{ if } -\frac{1}{g} < v_x < \frac{1}{g} \\ -1, \text{ if } v_x < -\frac{1}{g} \end{cases} \quad (1)$$

Energy Function In this case, the energy function can be written as

$$\begin{aligned} E &= -\frac{1}{2}\sum_{i,j}\sum_{C(k,l)\in N_r(i,j)} A(i,j;k,l)\, v_{yij}\, v_{ykl} + \frac{1}{2gR_x}\sum_{i,j}(v_{yij})^2 \\ &\quad - \sum_{i,j}\sum_{C(k,l)\in N_r(i,j)} B(i,j;k,l)\, v_{yij}\, v_{ukl} - \sum_{i,j} I_b v_{yij} \\ &= -\frac{1}{2}\mathbf{y}^T\left(\mathbf{A} - \frac{T_x}{g}\mathbf{I}\right)\mathbf{y} - \mathbf{y}^T\mathbf{b} = -\frac{1}{2}\mathbf{y}^T\mathbf{M}_g\mathbf{y} - \mathbf{y}^T\mathbf{b}. \end{aligned} \quad (2)$$

where the factor 1/g in the second term stems from the energy associated with the piecewise-linear function with a neuron gain other than unity. The dynamical equation remains unchanged except $\mathbf{y} = f_{pw}(g\,\mathrm{x})$ instead of $y = f_{pw}(\mathbf{x})$ Since $\mathbf{M}_g$ is also a real symmetric matrix, it can be diagonalized as $\mathbf{M}_g = A - (T_x/g)\mathbf{I} = Q\,\Lambda_g\mathbf{Q}^T$, where Λ_g is the diagonal matrix of eigenvalues λ_k. k =1, 2,, N, and Q is an N x N matrix whose columns are made of orthonormal set of eigenvectors e_k's.

Global Optimization and Stability in an annealed neural network, the elements of Λ_g are time-varying. However, Q is independent of the neuron gain because M and **Mg** commute. By noting that $\mathbf{M}_g = A - T_x\mathbf{I} - ((1-g)T_x/g)\mathbf{I} = M - ((1-g)T_x/g)\mathbf{I}$, the relationship between the eigenvalues of unannealed and annealed network can be easily shown to be

$$\lambda_k = \lambda'_k - \frac{(1-g)\,T_x}{g}, \quad k = 1, 2, \ldots, N \quad (3)$$

where λ_k's arc the eigenvalues of M. In the hardware annealing, the eigenvalues λ_k's are changed from all negative initial values to the final values λ_k's by increasing the neuron gain g, such that the energy

function (2) which is initially a convex function of y, is transformed gradually into a concave function. The initial neuron gain g_0 must be chosen such that $\lambda_k(g_0) < 0, \forall k$. The global optimization during this annealing process can be explained quantitatively [11]. Regardless of initial state values, the network results in the optimal solution at which its energy is minimized globally. The stability of the annealed CNN can also be proved by checking the behavior of $E(t)$ for $t \geq$ O [11]. Despite of the time-varying nature of the hardware annealing method, the stability of the network is still maintained as long as the gain control function $g = g(t)$ arc non-negative.

Dynamic Behavior The differential equation can be written as

$$C\frac{dx}{dt} = \mathbf{A}\ \mathbf{y} - T_x\ \mathbf{x} + \mathbf{b} \qquad (4)$$

where y = f(gx) and $\mathbf{b} = \mathbf{B}\ u + I_b\ w$ for a constant vector w = [1 1...1]^T. In (4), A and **B** are two-real N-by-N matrices determined by given cloning templates **TA** and **TB**, respectively. For the shift-invariant CNNs, they arc real symmetric. Initially, the gain g is small so that the network can be linearized. For the piecewise linear function, the assumption is exact until some of the neurons are saturated. In this case, Y = g x and (4) becomes $C\frac{dx}{dt} = \mathbf{M}_g\ x + \mathbf{b}$ where $\mathbf{M}_g = g\mathbf{A} - T_x\mathbf{I}$ for an N-by-N identity matrix I. The process of finding the optimal solutions takes place during the change of **Mg** from negative definite to indefinite matrix, as the annealing gain increases.

Simulation Results The edge detection results of a 64-by-64 CNN for unannealed and annealed conditions was presented in [11], The hardware annc.sling provides enough stimulation to those frozen neurons caused by such ill-conditioned initial states and gets better results.

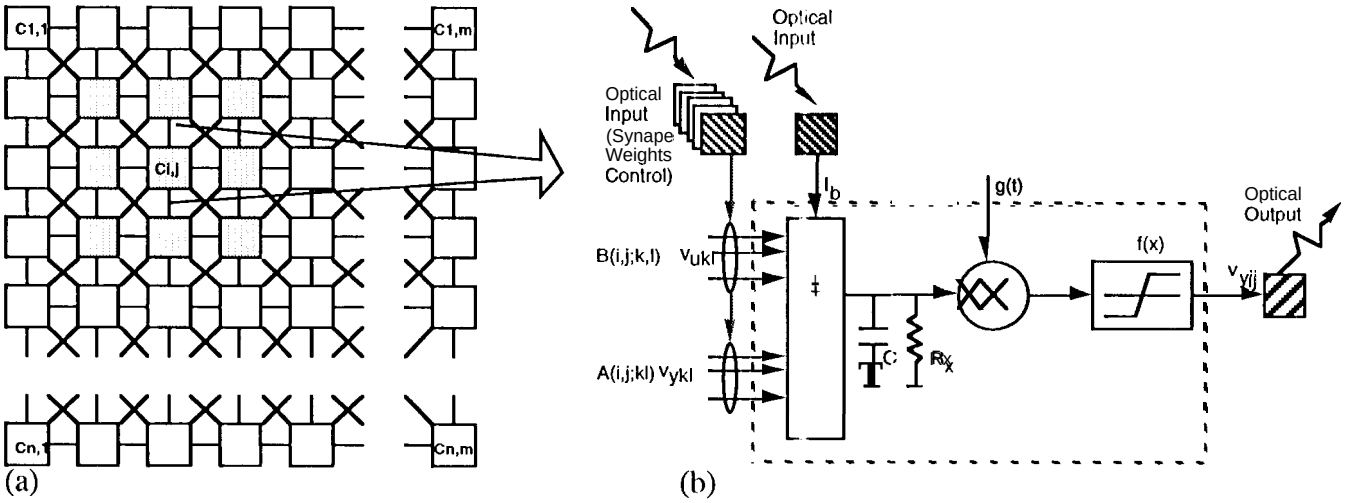


Fig. 3. (a) An n-by-m CNN on rectangular grid. The shaded boxes are the neighborhood cells of C(i,j). (b) Model of the CNN neuron C(i,j) with annealing and optical 1/0 capabilities.

2.2. Computing Architecture

The network considered in this design is a continuous-time, rectangular-type CNN with r= 1. A CNN unit consists of a core neuron cell, synaptic weights, input/output circuits, and digital interface, as shown in Fig. 4. To construct a complete CNN, a multiple of the units can be arranged in an n-by-m rectangular grid with appropriate interconnections. The digital interface provided are control data buses and read data lines. Four control buses for weights aO, al, a2, and bo arc 5-bit wide each. On the other

hand, a read data line is common to all the cells in a row, and a column select line is activated at a time to read cell outputs in a specific column. The data for synaptic weights are written into operator registers and the net work outputs arc fetched from the cell output latches. This method reduces the number of output signals and, because the read operations can take place during the next network operation without speed penalty in a moderate-siz,e network.

There are three kinds of feedback synaptic weights, aO, al and a2 and only one feedforward synapse in each ccl] for the direct input bo. If necessary, non-scalar TB may be implemented externally with bo = 1. The operator weight for bo can be configured as an independent programmable source with the input u connected to a fixed bias voltage. In other words, the input u can be written into the network through the digital interface; or a simple multilayer CNN can be realized in a time-multiplexed fashion. Depending on the applications, x(O) can be initialized to zero, a scaled v_u, or the weighted external inputs. One terminal of the capacitor C 1 is switched to the voltage x(0) during the initialization operation. At the same time, the outputs of the synapses go into the high-impedance state by control signal ϕ and $\bar{\phi}$, and the state node is connected to the ground to avoid possible spurious operation caused by the closed loop with the parasitic capacitance at the state node. In addition to the basic structure of the network, the annealing capability is provided to accommodate the applications in which the optimal solutions of energy function are required, The hardware annealing is performed by controlling the gain of the neuron, which is assumed to be the same for all neurons throughout the whole network. After the state is initialized to x = x(0), the initial gain at time t = O can be set to an arbitrarily small, positive value such that $0 < g(0) << 1$. It then increases continuously for $O < t < T_A$ to the nominal gain of 1. The maximum gain $g_{max} = 1$ is maintained for $T_A < t \leq T$, during which the network is stabilized. Note that the saturation level is still y = +1 or -1 and only the slope of f(x) around x = O varies,

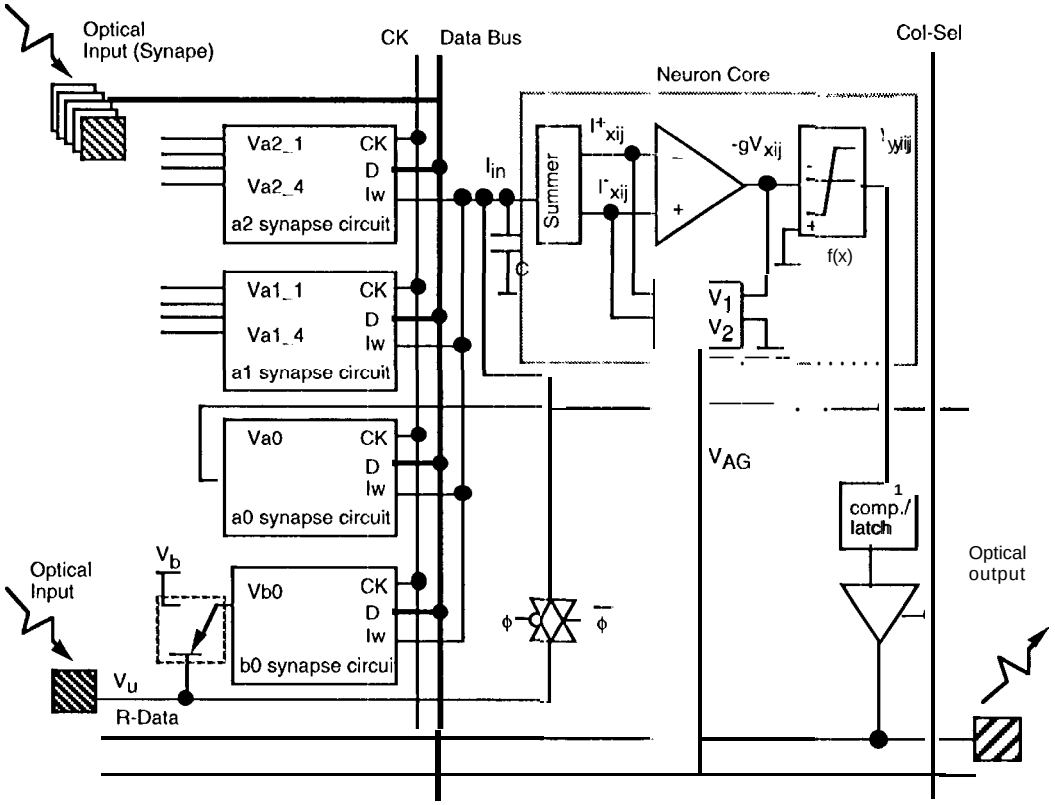


Fig. 4. A CNN unit consists of a core neuron cell, synaptic weights, 1/0 circuits, and digital interface.

2.3. Circuit Design

This section presents detailed circuit design for an annealed CNN neuron as shown in Fig. 4. To simplify the design, the current-mode approach [16,17] is used.

Programmable synapses: The circuit shown in Figure 5 is a binary-weighted current source array with the capability of four-quadrant multiplication, The magnitude of the multiplication is done by (n- 1) LSB bits and the polarity of the output I_W is controlled by swapping the inputs I_1 and 12 through the MSB bit. In this design, n = 5 and the sizes of transistors for weighting are chosen such that $|I_W| \leq (2 - 2^{-3})|I_{diff}|$, where $I_{diff} = I_1 - I_2$, in a step of 0.125 I_{diff}. Because the current mirrors are used several times, it is important to match them as closely as possible through a careful layout design. The synapse weight for the self-feedback *A(i, j; i, j)* must be a positive number greater than one. Thus, only four control bits are used for this synapse and, with the addition of constant factor of one, the range of output current is given by $I_d \leq I_W \leq (5 - 2^{-2})I_{diff}$ in a Step Of ().25 I_{diff}.

Transimpedance multiplier: The hardware annealing is performed by the premultiplication of the state v_{xij} by the gain control function g before the nonlinear function f( ) takes place. Special care must be taken in designing the circuit, because some analog multipliers often result in the post-multiplication $g \cdot f(v_{xij})$ as well as the desired function $f(g \cdot v_{xij})$. In other words, as the gain decreases, the linear operation region and saturation levels arc also reduced. In this case, the minimum gain $g_{in}i_n$ can not be made small arbitrarily. The basic element of the proposed circuit is the double-MOS differential resistor operating in triode region. When the double-MOS differential resistor is configured as the feedback resistor implemented with Ml 2-M 15, the following relation holds:

$$V_O = -(I^+ - 1-) / (mC_{ox})(W/L)(V_C - V_{DD}). \qquad (5)$$

Summing circuit: If the summation of the weighted currents from the neighboring cells is carried out directly in the transimpedance multiplier, the value of resistance Rx is inversely proportional to the gain-control voltage V_c. In order to accommodate a constant Rx, the constant input impedance current inverter implemented with M 1-MS as shown in Fig. 6 can be used at the input stage of the multiplier.

Nonlinear function: The circuit for the nonlinear function y = f(x) is accomplished by a simple transconductor consisting of a differential amplifier. Its large signal transfer function is a smooth, sigmoid-like characteristics. A weak positive feedback is applied to increase the transconductance value without increasing the (W/L) ratio of the differential-pair transistors M 17 and M 18. The transistors M20 - M22 in saturation determine the feedback factor $\alpha, 0 \leq \alpha \leq 1$,

$$\alpha = (W/L)_{M21}/(W/L)_{M20} = (W/L)_{M23}/(W/L)_{M22} \qquad (6)$$

Then, the transconductance at $V_d = V_O - V_G = 0$ is shown to be $g_m = g_m(\alpha=0)/(1-\alpha)$.

2.4. Chip Implementation

A annealed CNN chip with 5x5 neural cells is designed and fabricated in a 2.0 mm CMOS technology through MOSIS Services. The die photo is shown in Fig. 7.

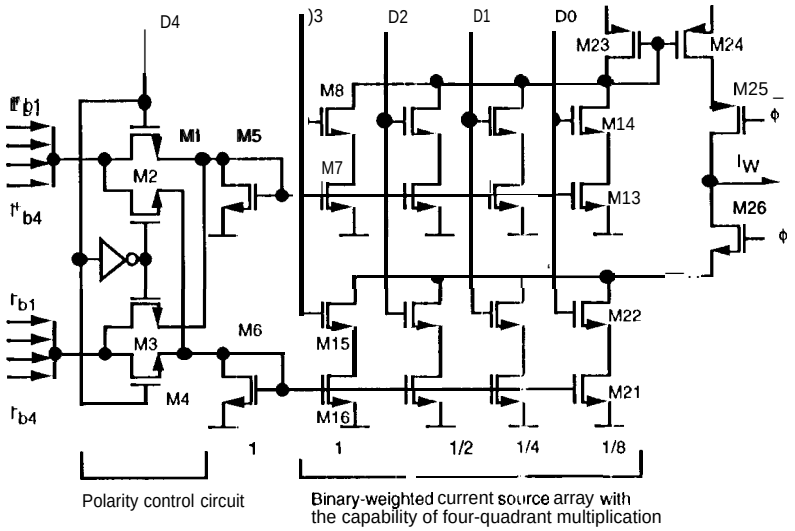


Fig. 5. Detailed circuitry of a digitally programmable synaptic weights.

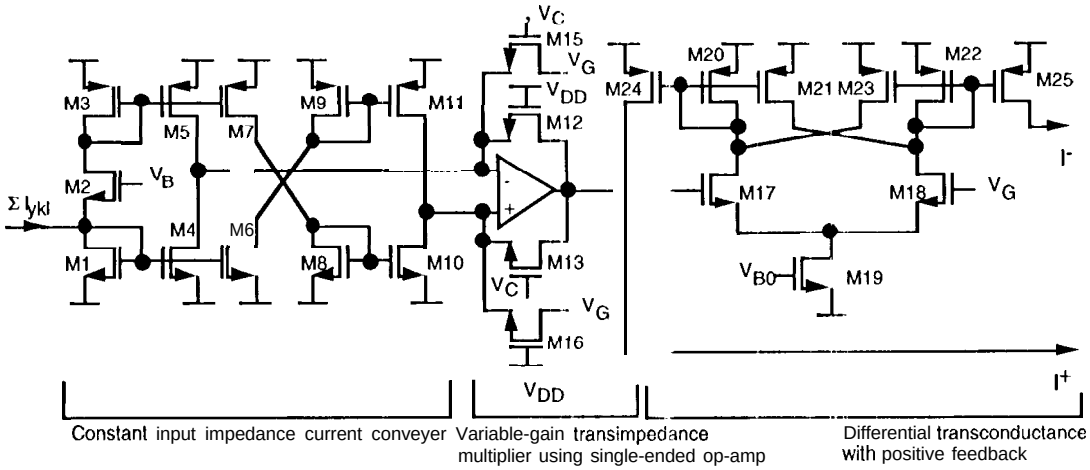
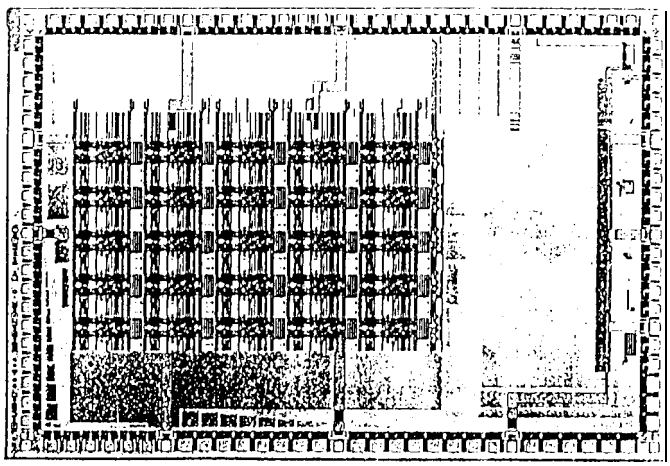


Fig. 6 Detailed circuitry of a variable-gain cell.



Fig, 7, Die photo of the annealed CNN chip with 5x5 neural cells.

3. A MONOLITHIC GaAs 2-D ARRAY OF OPTICAL RECEIVERS

A 2-D array of the optical receivers and receivers can be compactly implemented in a single GaAs chip for high-speed interconnection networks and photonic signal processing. The key engineering design challenge is due to the fact that the front-end unit of the receiver needs to operate at a very high rate and at a very low noise level while the following signal processing units require the high-speed operation which could generate a large switching noise. The GaAs MESFET technology becomes a suitable candidate for this type of integration because various circuits can be integrated onto a single chip as fabrication technologies become more mature for large-volume production [18].

The optical receiver which includes the photodetector and preamplifier was designed and fabricated using a common 1.0 μm gallium-arsenide MESFET technology provided by the Vitesse Semiconductor Corp. through MOSIS Service. Since this technology is usually aimed for high-speed digital logic circuits. The main purpose of this work is to optimize the high-performance optical receiver design based upon this common fabrication technology without any modification in the processing steps. This regular fabrication technology can provide both the depletion (D)-mode and the enhancement (E)-mode transistors. However, design methodology using the all D-mode transistors is chosen for better component uniformity throughout the processing clement array.

3.1. Design of An Optical Receiver

The detailed circuit schematic of an optical receiver using the transimpedance (TZ) amplifier is shown in Fig. 8. It consists of a photodetector, a preamplifier, and the feedback resistance. Depletion-mode MESFET's with a minimum gate length of 1.0 μm are used for all the transistors except the feedback transistor Z7. Several design factors should be carefully addressed to optimize receiver performances such as the bandwidth, noise characteristics, dynamic range, and power consumption.

Photodetector A simple, planar n~etal-semiconductor-metal (MSM) diode structure is used for photodetector, In contrast to the case of the conventional p-i-n diode, the associated parasitic capacitance in a MSM photodetector is significantly reduced because the electrode is not directly connected to the substrate. Such a property is extremely crucial to the speed and noise characteristics.

Preamplifier The voltage amplifier consists of transistors Z1 through Z6 and the diodes D] and D2. The voltage gain results from the input gain stage of Zl and Z2, providing the DC gain of 22 dB. The level-shifting stage consists of transistors Z3, Z4, and diodes. The output buffer consists of transistors Z5 and Z6. Sizes of the transistors arc determined so that the output impedance is matched to 50 Ohm.

Feedback Resistance A passive resistor made from the diffusion region can possess a large parasitic capacitance. Therefore, the feedback resistance is implemented by an active transistor biased in the triode region. In addition, the resistance value can be continuously tunable in order to satisfy different application specifications. The W/L ratio of this feedback transistor is 10/6 pm, which can realize the resistance value of 1 to 10K Ohms with a control on the gate voltage.

3.2. Design Analysis and Simulation

Assume that the open-loop voltage transfer has the DC voltage gain of $A_V(0)$ and the 2-dB frequency of $1/(2\pi R_o C_o)$. Here, R. and C_o are the output resistor and capacitor, respectively, which determine the dominant pole of the open-loop voltage amplifier. The bandwidth of the closed-loop transfer function can be expressed as

$$f_{3dB} = 1/(2\pi\tau_p). \quad (7)$$

and τ_p consists of three RC-products as follows:

$$\tau_p = R_{eq,CPD+CIP}(C_{PD} + C_{IP}) + R_{eq,CFB}C_{FB} + R_{eq,Co}C_o \quad (8)$$

where the Req is the equivalent Thevenin resistance of each capacitor. By calculating the value of the equivalent Thevenin resistance, t , can be obtained as

$$\tau_p = (R_o + R_{FB})(C_{PD} + C_{IP})/(1+A_V(0)) + R_{FB}C_{FB} + (R.C_o)/(1+A_V(0)) \quad (9)$$

Here, C_{PD} and C_{IP} are the parasitic capacitances of the photodetector and the input node of the amplifier, respectively. The parasitic capacitance C_{FB} is associated with the feedback resistance R_{FB}. The value of C_{IP} is proportional to the product of the unit gate-source capacitance and the width of the transistor Z1.

The squared input equivalent noise current operating at the bit rate B can be expressed as [19]

$$\langle i_n^2 \rangle = 2q(I_D + I_L)I_2B + 4kTI_2B/R_{FB} + 8kT\Gamma(2\pi C_T)^2 f_c I_f B2 / g_m + 4kT\Gamma(2\pi C_T)^2 I_3 B^3 / g_m \quad (10)$$

Here, q is the electronic charge, k is the Boltzmann's constant, T is the absolute temperature, I_D is the dark current of the photodiode, I_L is the leakage current of the transistor, g_m is the transconductance parameter of the transistor, Γ is the transistor noise figure, f_C is the l/f noise corner frequency, 12, I_3, and If are the effective receiver bandwidth integrals. The total parasitic capacitance C_T at the input node is contributed by the photodetector, input transistor, and feedback transistor.

The bandwidth and noise characteristics of the optical receiver with respect to the value of the feedback resistance R_{FB} and the width of the input transistor W 1 are shown in Fig. 9. The minimum R_{FB} is determined from the equivalent input noise current and the maximum value is determined from the achievable bandwidth. One W1-value corresponds to the minimum input noise current because both C_T and gill in (10) are proportional to the value of W 1. The low data rate, small power-line inductance, and small power supply voltages are key factors in reducing the coupling noises. In order to integrate a large array of optical receivers on a single IC chip, capacitive coupling noise and thermal noise should be minimized for maximum receiver sensitivity [20]. In addition, the switching noise from the digital circuitry incorporating the postprocessing functions should be shielded to avoid coupling into the power supply lines.

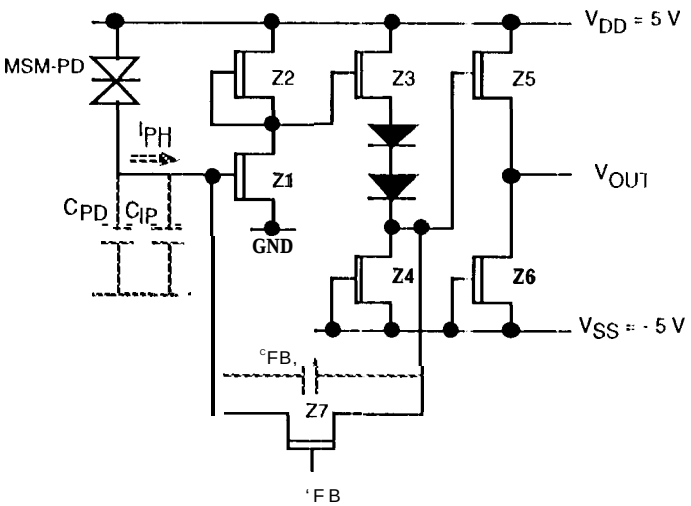
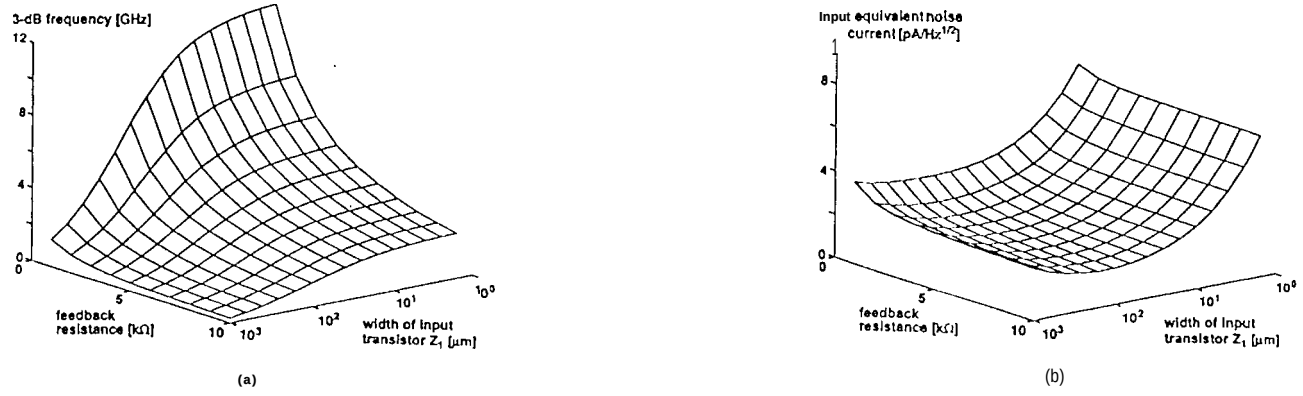


Fig. 8. Circuit schematic of the optical receiver using the TZ amplifier.

3.3. Implementation and Measurement

Die photo of the optical receiver is shown in Fig. 10, which occupies an area of 220 x 72 μm^2. Fig. 2-5 shows the measurement results of the MSM photodetector. An interleaved-digit type gate metal is used with each finger width of 1.0 μm and spacing between fingers of 1.2 pm. The estimated parasitic capacitance of a 20x20-μm^2 photodetector is around 0.1 pF. The wavelength of the laser diode in the measurement setup is 0.88 μm with the optical power of 15 μW. In the operating range with the detector bias voltage of 5 V, the dark current is smaller than 10 nA. The quantum efficiency of the photodiode is 35%-40% and the measured sensitivity is 0.27-0.35 A/W. By adjusting the gate voltage applied to the feedback transistor, the transimpedance value can be modified. Fig. 12 shows the measured results and the corresponding simulation results on the characteristics of the tunable transimpedance value. Fairly good agreement between measured data and simulated results is achieved. This TZ amplifier can have a tunable transimpedance value between 1 and 10k Ohms.



Fig, 9. Bandwidth (a) and noise characteristics (b) of the designed optical receiver. Here C_{PD} = 0.1 pF.

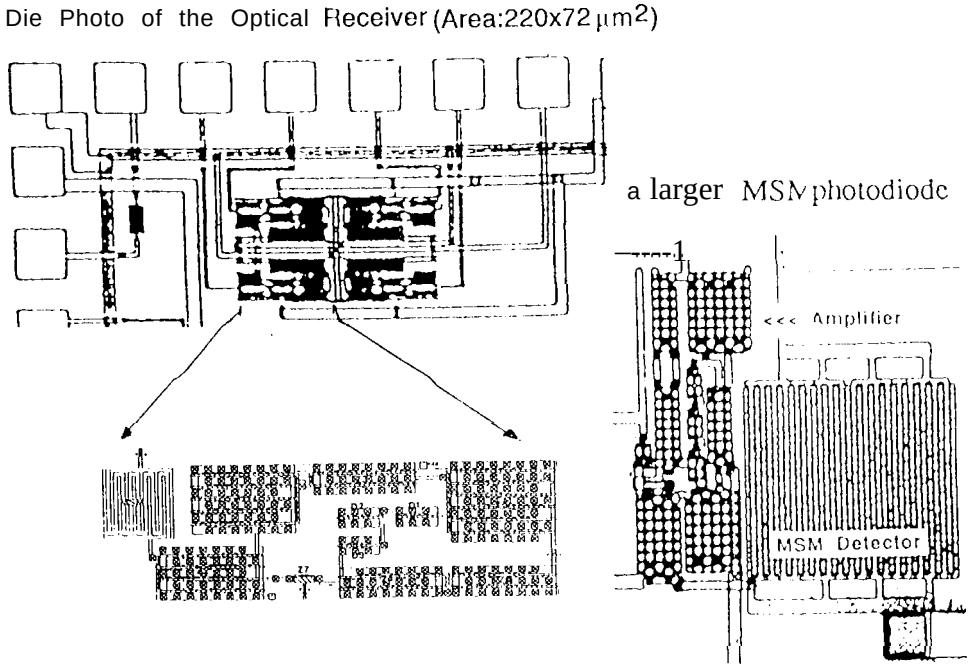
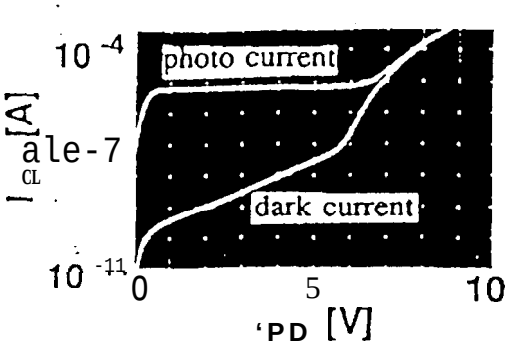


Fig. 10. Die photo of the optical receivers array



Fig, 11 Measurement results of the MSM photodetector.

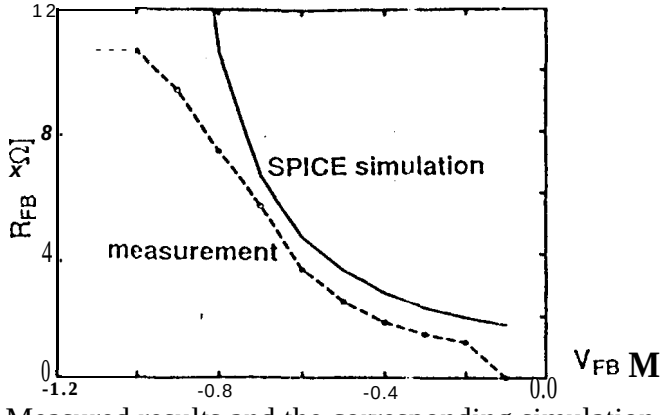


Fig. 12 Measured results and the corresponding simulation results on the characteristics of the tunable transimpedance.

4. CONCLUSIONS

A 2-D array of the integrated optical receivers and smart pixels can be compactly implemented in a single flip-chip connected multi-chip module for high-speed interconnection networks and photonic signal processing,

A monolithic GaAs 2-D array of optical receivers was designed and fabricated using a common 1.0 μm gallium-arsenide MESFET technology. The optical receiver operates at the data rate of 1 Gb/s. The transimpedance value can be continuously tuned from 1 to 10k Ohms. The metal-semiconductor-metal photodiode shows a 35% efficiency. Several design factors are considered to achieve high-bandwidth and low-noise operation.

The smart pixel design is based on cellular neural network with annealing ability. Local interconnection and simple synaptic operators are the most attractive features of the CNN for VLSI implementation in high-speed, real-time applications. The CMOS VLSI design of a continuous-time shift-invariant CNN with digitally-programmable operators is presented. The circuits with hardware annealing is included to achieve optimal solutions in a variety. of applications.

The proposed compact 2-D array of integrated optical receivers and smart-pixel chips can take the combined advantages of the optics and electronics and achieve high-speed computer communication and signal processing.

5. ACKNOWLEDGMENTS

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CLEARANCE NO._71_____

PREPUBLICATION REVIEW RECORD

INSTRUCTION: Check statement of circumstances applicable to this clearance and indicate action taken.

APPLICABLE CIRCUMSTANCE(S):

1. ( ) A JPL "reportable item" is not disclosed but may exist or be "in the making." (NOTE: Originate Notice of Ncw Technology).

2, (XX) JPL or ( ) JPL SubK unreported "reportable item" is disclosed, (NOTE: Originate Notice of Ncw Technology - if SubK, request NTR and decline clearance until NTR is received. Caltech and NRO to review for foreign filing when "item" is within a statutory class of patentable subject matter).

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CLEARANCE: ( ) Recommended ( ) Conditional - see Comments ( ) Delayed - see Comments

COMMENTS: **Two chip designs based on the continuous-time, shift-invariant cellular neural nerwork** disclosed in Clearance No. 69 **(Mar.).**

PREPARED BY: R.L. Klein March 16.1995